MAX3663ETG Input Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Component*s.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Revision A0, August 31, 2004

Input Model for the MAX3663

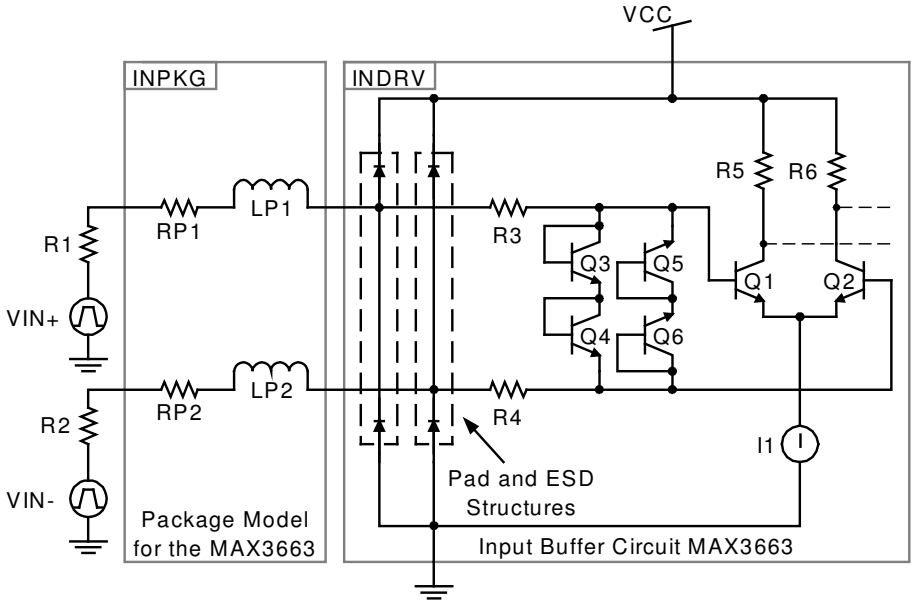

Figure 1. Input Model for signal DATA of the MAX3663.

Notes:

The schematics on the previous page represent the output and input stage of the Maxim MAX3663 622Mbps Laser Driver. The input circuit is shown with the signal inputs (DATA+, DATA-). However, the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note (HFAN-06.3), the input signals are described as (2101, 2102). These models are only valid at 25°C. The bias currents for the input circuitry are modeled by ideal current sources. This model is not compensated for variations in VCC, so VCC equal to 3.3V should be used.

The Input Stage: The input stage has sub-circuits "INDRV" and "INPKG".

The INDRV Sub-circuit: The input package connects to a differential pair. The signal continues through the input buffer from nodes 4 and 5 (positive and negative nodes respectively). To set a certain V_{ID}, you need to choose the input voltage. The range for V_{ID} is 200mV to 1600mV. See the input netlist on instructions to do this. The driving voltage source should be set to 0V differential at t=0. This ensures that the two AC coupling capacitors are not charged to different voltages initially (this is the way the circuit operates in steady-state operation). This was achieved by using a piecewise linear source as the driver. See Appendix A for the input netlist.

Text File Format: This model is shipped in "pdf" format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the "Text Select Tool." Then the user can "select" what netlist and/or subcircuit with the mouse. Then use the copy command from the "edit" menu to capture the selected lines. These lines can then be "pasted" into the user's text file.

Appendix A: Input Netlist

```
* 3663 Input Model
**********************************************
.OPT ACCT NOMOD LIMPTS=10000
.TEMP 25
.OP
.TRAN 2P 4n
**********************************************

* Voltage Source
VCC 101 0 3.3V

**********************************************
*  Add input source here.
*  The source should connect to node 50 (VINP)
*  and 60 (VINN).
*  Example:

* For VID of 200mV and VINCM of VCC-VIN/4 (3.25V)
VINP  50 0 PULSE (3.3 3.2 .1n 100p 100p 1.5n 3.21543n)
VINN  60 0 PULSE (3.2 3.3 .1n 100p 100p 1.5n 3.21543n)
* For VID of 800mV and VINCM of 1.98V
*VINP  50 0 PULSE (2.38 1.62 .1n 100p 100p 1.5n 3.21543n)
*VINN  60 0 PULSE (1.62 2.38 .1n 100p 100p 1.5n 3.21543n)
* For VID of 1600mV and VINCM of 1.81V
*VINP  50 0 PULSE (2.21 1.41 .1n 100p 100p 1.5n 3.21543n)
*VINN  60 0 PULSE (1.41 2.21 .1n 100p 100p 1.5n 3.21543n)

R1 50 2101 50
R2 60 2102 50
**********************************************

**********************************************
XINPKG 2101 2102 600 601 INPKG
XINDRV 600 601 101 INDRV
**********************************************

**********************************************
.SUBCKT INDRV 600 601 101

R3 600 800 250
R4 601 801 250
R5 4 101 1k
R6 5 101 1k
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```
* Clamp
XQ3 600 600 400 0 H21M022
XQ4 400 400 601 0 H21M022
XQ5 601 601 401 0 H21M022
XQ6 401 401 600 0 H21M022

* Differential Pair
XQ1 5 800 3 0 H21M022
XQ2 4 801 3 0 H21M022

I1 3 0 .2mA

* ESD Diodes
XD1 600 101 0 HDE072021
XD2 0 600 0 HDE072021
XD3 601 101 0 HDE072021
XD4 0 601 0 HDE072021

* Pad Structures
XP1 600 0 HPAD3
XP2 601 0 HPAD3

.ENDS INDRV
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.SUBCKT INPKG 2101 2102 600 601

RP1 2101 500 14.4m
RP2 2102 501 14.4m
LP1  500 600 .324n
LP2  501 601 .324n

.ENDS INPKG
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* Transistor Model
.SUBCKT H21M022 1 2 3 21
CP1EPI 1 2 1.057F
CP1P2 12 3 2.077F
CTRENCH 1 20 4.783F
RBX 2 12 258.128 TC=2.875M
RCX 1 10 149.813 TC=3.067M,1.773U
RCI 10 11 7.885 TC=3.067M,1.773U
REX 13 3 28.450 TC=61.009U
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```
RSUB 20 21 26.178K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=2.881E-018 XTI=3 EG=1.140 BF=245.919 BR=20 XTB=450M
+   VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=10.808M
+   IKR=198U ISE=1.362E-021 ISC=1.752E-030 RB=258.128 RBM=193.596
+   IRB=1.752M CJE=9.312F MJE=490M VJE=940M FC=990M CJC=2.167F
MJC=470M
+   VJC=850M TF=3.651P TR=19N XTF=1 VTF=1K ITF=5.351M PTF=5 KF=1.500F
+   AF=1 )
.MODEL TXP PNP( IS=2.016E-019 CJE=2.167F MJE=470M VJE=850M CJC=3.870F
+   MJC=400M VJC=650M BF=10K BR=797.721U TF=1N FC=900M )
.ENDS H21M022
************************************************

************************************************
* Pad Model
.SUBCKT HPAD3 1 3
CPAD 1 10 86.407F
REPI 10 20 149.204M TC=4.800M,5U
CTRENCH 21 20 79.795F
DS 21 20 DSUB
RS 3 21 369.115
.MODEL DSUB D( IS=98.719F CJO=555.750F M=400M VJ=650M )
.ENDS HPAD3
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* Diode Model
.SUBCKT HDE072021 1 2 21
CP1EPI 1 4 20.699F
QD 5 4 1 5 QESD
RS 4 2 9.056 TC=3.090M,2.439U
RSUB 5 21 7.145K
CTRENCH 2 5 12.437F
.MODEL QESD PNP( IS=2.591E-018 NF=1.050 BF=800M BR=600U CJE=34.006F
+   VJE=600M MJE=400M CJC=18.342F VJC=650M MJC=400M )
.ENDS HDE072021
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.PROBE
.END
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